Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.066”**

**1**

**2**

**3**

**.066”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .0055” X .0055”**

**Backside Potential: GND or leave FLOATING**

**Mask Ref: MO01-2**

**APPROVED BY: DK DIE SIZE .066” X .066” DATE: 8/1/17**

**MFG: MOTOROLA THICKNESS .015” P/N: MCC7806AC**

**DG 10.1.2**

#### Rev B, 7/1